# 16-Bit, 600+ MSPS D/A Converter

Preliminary Technical Data

# AD9726

## FEATURES

600+ MSPS DAC update rate
16/14/12/10-bit resolution family
LVDS interface with built-in 100-termination resistors
Single data rate and double data rate capability
Excellent dynamic performance
SFDR = 65 dBc at 140 MHz
IMD = 75 dBc at 140 MHz
Differential current outputs: 2 mA to 20 mA
–40°C to +85°C temperature range operation
On-chip 1.20 V reference
Package: 80-lead thermally-enhanced TQFP
Versatile clock and data interface

## APPLICATIONS

Instrumentation and test
Wideband communications systems
Point-to-point wireless
LMDS
PA linearization
High resolution displays

## FUNCTIONAL BLOCK DIAGRAM

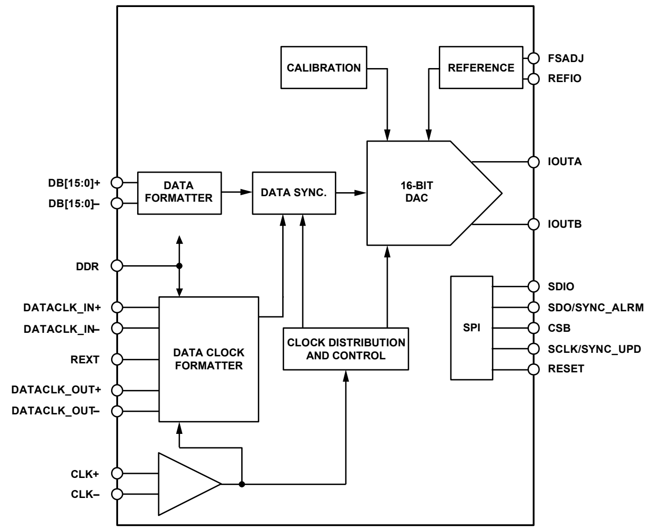


*Figure 1*

## PRODUCT DESCRIPTION

The AD9726 is a 16-bit digital-to-analog converter (DAC) that utilizes an LVDS interface to achieve conversion rates in excess of 600 MSPS. It is in a family of pin compatible converters that offers selection of 10-bit, 12-bit, 14-bit, and 16-bit resolution grades. All of the devices share the same interface options, small outline package, and pinout, providing an upward or downward component selection path based on performance, resolution and cost.

## PRODUCT HIGHLIGHTS

Ultralow noise and intermodulation distortion (IMD) enable high quality waveform synthesis at intermediate frequencies up to 200 MHz.

LVDS receivers support SDR or DDR modes, with the maximum conversion rate exceeding 600 MSPS.

Manufactured on a CMOS process, the AD9726 uses a proprietary switching technique that enhances dynamic performance.

The current output of the AD9726 can be easily configured for various single-ended or differential circuit topologies.

**Rev. PrD**


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| Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|
| Resolution | 16 | | | Bits |
| DC Accuracy | | | | |
| Integral Nonlinearity | | ±1.5 | | LSB |
| Differential Nonlinearity | | ±0.75 | | LSB |
| Analog Output | | | | |
| Offset Error | –1 | | 1 | %FSR |
| Gain Error | | | | %FSR |
| Full Scale Output Current | | 20 | 1.26 | mA |
| Output Compliance Range | 1.14 | | | V |
| Output Resistance | | TBD | 1.25 | kW |
| Output Capacitance | 0.1 | TBD | | pF |
| Reference Output | | | | |
| Reference Voltage | | 1.2 | | V |
| Reference Output Current | | 100 | | nA |
| Reference Input | | | | |
| Reference Input Compliance Range | | | | V |
| Reference Input Resistance | | 5 | | kW |
| Small Signal Bandwidth | | 0.5 | | MHz |
| Temperature Coefficients | | | | |
| Offset Drift | | TBD | | ppm of FSR/°C |
| Gain Drift (With Internal Reference) | | TBD | | ppm of FSR/°C |
| Reference Voltage Drift | | TBD | | ppm/°C |
| Power Supply[1] | | | | |
| AVDD1, AVDD2 | | | | |
| Voltage Range | | 3.3 | | V |
| Analog Supply Current ($I_{AVDD1} + I_{AVDD2}$) | | 51 | | mA |
| ADVDD | | | | |
| Voltage Range | | 2.5 | | V |
| ACVDD | | | | mA |
| Voltage Range | | 2.5 | | V |
| Analog Supply Current ( $I_{ADVDD} + I_{ACVDD}$) | | 9 | | mA |
| CLKVDD | | | | |
| Voltage Range | | 2.5 | | V |
| Clock Supply Current ($I_{CLKVDD}$) | | 20 | | mA |
| DVDD | | | | |
| Voltage Range | | 2.5 | | V |
| Digital Supply Current ($I_{DVDD}$) | | 69 | | mA |
| DBVDD | | | | |
| Voltage Range | | 3.3 | | V |
| Digital Supply Current ($I_{DBVDD}$) | | 20 | | mA |
| Nominal Power Dissipation ($P_{DIS}$)[2] | | 479 | | mW |
| Nominal Power Dissipation ($P_{DIS}$)[3] | | 1000 | | mW |

[1]Supply currents measured under the following conditions: $f_{DAC}$ = 200 MSPS, $f_{OUT}$ = 11 MHz, nominal power supply voltages
[2]Power dissipation measured under the following conditions: $f_{DAC}$ = 200 MSPS, $f_{OUT}$ = 11 MHz, nominal power supply voltages
[3]Power dissipation measured under the following conditions: $f_{DAC}$ = 600 MSPS, $f_{OUT}$ = 111 MHz, nominal power supply voltages

## AC SPECIFICATIONS

**Table 2. $T_{MIN}$ to $T_{MAZ}$, AVDD1, AVDD2, DBVDD = 3.3 V, ADVDD, ACVDD, CLKVDD, DVDD = 2.5 V, $I_{OUTFS}$ = 20 mA, unless otherwise noted. Specifications subject to change without notice.**

| Parameter | Typ | Unit |
|---|---|---|
| Dynamic Performance | | |
| Max DAC Output Update Rate (DDR) | 600 | MSPS |
| Max DAC Output Update Rate (SDR) | 440 | MSPS |
| AC Linearity | | |
| Spurious Free Dynamic Range (SFDR) to Nyquist ($f_{OUT}$ = 0 dBFS) | | |
| $f_{DATA}$ = 260 MSPS, $f_{OUT}$ = 20 MHz | 71 | dBc |
| $f_{DATA}$ = 260 MSPS, $f_{OUT}$ = 70 MHz | 68 | dBc |
| $f_{DATA}$ = 260 MSPS, $f_{OUT}$ = 120 MHz | 68 | dBc |
| $f_{DATA}$ = 400 MSPS, $f_{OUT}$ = 20 MHz | 72 | dBc |
| $f_{DATA}$ = 400 MSPS, $f_{OUT}$ = 70 MHz | 66 | dBc |
| $f_{DATA}$ = 400 MSPS, $f_{OUT}$ = 140 MHz | 60 | dBc |
| $f_{DATA}$ = 600 MSPS, $f_{OUT}$ = 20 MHz | TBD | dBc |
| $f_{DATA}$ = 600 MSPS, $f_{OUT}$ = 125 MHz | TBD | dBc |
| $f_{DATA}$ = 600 MSPS, $f_{OUT}$ = 250 MHz | TBD | dBc |
| Two Tone IMD to Nyquist ($f_{OUT1}$ = $f_{OUT2}$ = −6 dBFS) | | |
| $f_{DATA}$ = 300 MSPS, $f_{OUT1}$ = 26 MHz, $f_{OUT2}$ = 27 MHz | 89 | dBc |
| $f_{DATA}$ = 300 MSPS, $f_{OUT1}$ = 100 MHz, $f_{OUT2}$ = 101 MHz | 80 | dBc |
| $f_{DATA}$ = 300 MSPS, $f_{OUT1}$ = 126 MHz, $f_{OUT2}$ = 127 MHz | 80 | dBc |
| $f_{DATA}$ = 500 MSPS, $f_{OUT1}$ = 26 MHz, $f_{OUT2}$ = 27 MHz | 90 | dBc |
| $f_{DATA}$ = 500 MSPS, $f_{OUT1}$ = 100 MHz, $f_{OUT2}$ = 101 MHz | 78 | dBc |
| $f_{DATA}$ = 500 MSPS, $f_{OUT1}$ = 126 MHz, $f_{OUT2}$ = 127 MHz | 76 | dBc |
| $f_{DATA}$ = 600 MSPS, $f_{OUT1}$ = 26 MHz, $f_{OUT2}$ = 27 MHz | TBD | dBc |
| $f_{DATA}$ = 600 MSPS, $f_{OUT1}$ = 126 MHz, $f_{OUT2}$ = 127 MHz | TBD | dBc |
| $f_{DATA}$ = 600 MSPS, $f_{OUT1}$ = 250 MHz, $f_{OUT2}$ = 251 MHz | TBD | dBc |
| Noise Spectral Density (NSD) | | |
| $f_{DATA}$ = 500 MSPS, $f_{OUT}$ = 20 MHz, 0 dBFS | −162 | dBm/Hz |
| $f_{DATA}$ = 500 MSPS, $f_{OUT}$ = 20 MHz, −12 dBFS | −165 | dBm/Hz |
| $f_{DATA}$ = 500 MSPS, $f_{OUT}$ = 120 MHz, 0 dBFS | −151 | dBm/Hz |
| $f_{DATA}$ = 500 MSPS, $f_{OUT}$ = 120 MHz, −12 dBFS | −161 | dBm/Hz |
| CDMA2000 Adjacent Channel Leakage Ratio (ACLR) | | |
| $f_{DATA}$ = 245.76 MSPS, IF = 61.44 MHz | TBD | dBc |
| $f_{DATA}$ = 491.52 MSPS, IF = 122.88 MHz | TBD | dBc |
| $f_{DATA}$ = 491.52 MSPS, IF = 190 MHz | TBD | dBc |
| WCDMA Adjacent Channel Leakage Ratio (ACLR), Single Carrier | | |
| $f_{DATA}$ = 184.32 MSPS, IF = 61.44 MHz | 79 | dBc |
| $f_{DATA}$ = 245.76 MSPS, IF= 61.44 MHz | 79 | dBc |
| $f_{DATA}$ = 491.52 MSPS, IF = 122.88 MHz | 76 | dBc |
| $f_{DATA}$ = 491.52 MSPS, IF = 190 MHz | 74 | dBc |
| WCDMA Adjacent Channel Leakage Ratio (ACLR), Four Carrier | | |
| $f_{DATA}$ = 184.32 MSPS, IF = 61.44 MHz, | 69 | dBc |
| $f_{DATA}$ = 368.64 MSPS, IF = 92.16 MHz | 67 | dBc |

## DIGITAL SPECIFICATIONS

**Table 3. $T_{MIN}$ to $T_{MAX}$, AVDD1, AVDD2, DBVDD = 3.3 V, ADVDD, ACVDD, CLKVDD, DVDD = 2.5 V , $I_{OUTFS}$ = 20 mA, unless otherwise noted. Specifications subject to change without notice.**

| Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Digital Inputs | VCM = 0.875 V to 1.575 V | | | | |
| Differential Logic '1' | (put into footnote, and delete column?) | 0.1 | | 0.6 | V |
| Differential Logic '0' | | –0.6 | | –0.1 | V |
| Logic '1' current | | | 3.5 | | mA |
| Logic '0' current | | | 3.5 | | mA |
| Differential Input Resistance | | | 100 | | W |
| Differential Input Capacitance | | | 3 | | pF |
| Data Setup Time ($t_{DS}$) | | | 0.9 | | ns |
| Data Hold Time ($t_{DH}$) | | | –0.3 | | ns |
| Data Clock Output Delay ( $t_{DCO}$) | | | 2.4 | | ns |
| Serial Control Bus | | | | | |
| Maximum SCLK Frequency (fSCLK) | | 15 | | | MHz |
| Minimum Clock Pulse Width High ($t_{PWH}$) | | 30 | | | ns |
| Minimum Clock Pulse Width Low ($t_{PWL}$) | | 30 | | | ns |
| Maximum Clock Rise/Fall Time | | | | 1 | ms |
| Minimum Data/Chip Select Set Up Time ($t_{DS}$) | | 25 | | | ns |
| Minimum Data Hold Time ($t_{DH}$) | | 0 | | | ns |
| Maximum Data Valid Time ($t_{DV}$) | | | | 30 | ns |
| RESET Pulse Width | | 1.5 | | | ns |
| Inputs (SDI, SDIO, SCLK, CSB) | | | | | |
| Logic '1' Voltage | | 2.1 | 3 | | V |
| Logic '0' Voltage | | | 0 | 0.9 | V |
| Logic '1' Current | | –10 | | +10 | µA |
| Logic '0' Current | | –10 | | +10 | µA |
| Input Capacitance | | | 5 | | pF |
| SDIO Output | | | | | |
| Logic '1' Voltage | | DRVDD–0.6 | | | V |
| Logic '0' Voltage | | | | 0.4 | V |
| Logic '1' Current | | 30 | | 50 | mA |
| Logic '0' Current | | 30 | | 50 | mA |

## DIGITAL TIMING INFORMATION

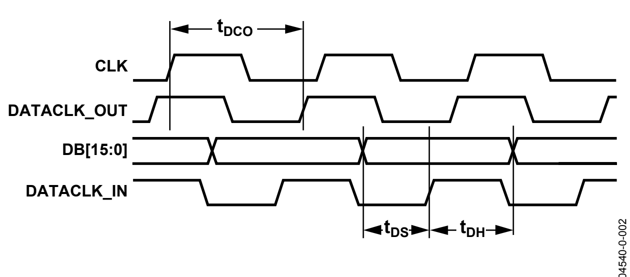


*Figure 2. Single Datarate (SDR) Mode*

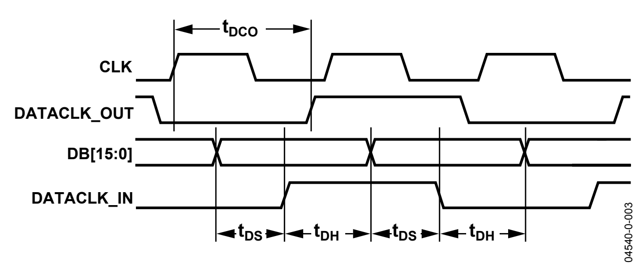


*Figure 3. Double Datarate (DDR) Mode*

# ABSOLUTE MAXIMUM RATINGS

| Parameter | With Respect to | Min | Max | Unit |
|---|---|---|---|---|
| AVDD1, AVDD2, DBVDD | ACOM1, ACOM2, DBCOM | −0.3 | TBD | V |
| ADVDD, ACVDD, CLKVDD, DVDD | ADCOM, ACCOM, CLKCOM, DCOM | −0.3 | TBD | V |
| ACOM1, ACOM2, DBCOM | ACOM1, ACOM2, DBCOM | −0.3 | +0.3 | V |
| ADCOM, ACCOM, CLKCOM, DCOM | ADCOM, ACCOM, CLKCOM, DCOM | −0.3 | +0.3 | V |
| REFIO, FSDAJ | ACOM1 | −0.3 | AVDD1 + 0.3 | V |
| IOUTA, IOUTB | ACOM1 | −1 | AVDD1 + 0.3 | V |
| DB0-DB15, DB0-DB15 | DBCOM | −0.3 | DBVDD + 0.3 | V |
| DATACLKOUT, DATACLKOUT | DBCOM | −0.3 | DBVDD + 0.3 | V |
| REXT, CLK+, CLK- | CLKCOM | −0.3 | CLKVDD + 0.3 | V |
| SDO/SYNC_ALRM, SDIO, CSB | DBCOM | −0.3 | DBVDD + 0.3 | V |
| SCLK/SYNC, RESET | DBCOM | −0.3 | DBVDD + 0.3 | V |
| DDR, SPI_DIS | ADCOM | −0.3 | ADVDD + 0.3 | V |

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

# PIN CONFIGURATION AND FUNCTION DESCRIPTION

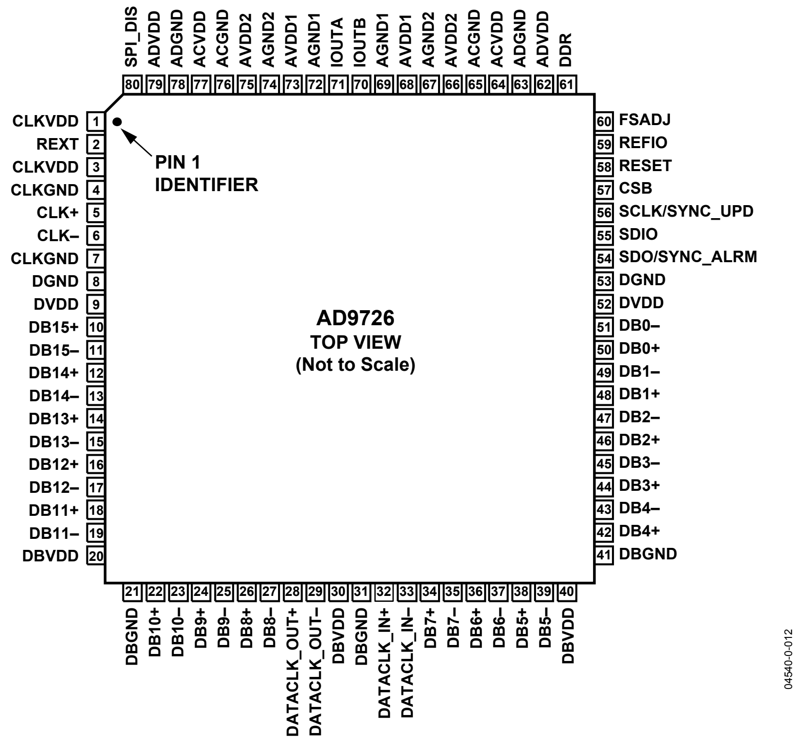


*Figure 4. Pin Configuration*

**Table 4. Pin Function Description**

| Pin No. | Name | Description | Pin No. | Name | Description |
|---|---|---|---|---|---|
| 1 | CLKVDD | Clock Supply Voltage | 41 | DBGND | Digital Data Supply Common |
| 2 | REXT | Bias Resistor. Sets DATACLK_OUT drive strength. Nominally 1 kΩ to DBGND | 42 | DB4+ | Digital Input Bit 4–True |
| 3 | CLKVDD | Clock Supply Voltage | 43 | DB4– | Digital Input Bit 4–Complement |
| 4 | CLKGND | Clock Supply Common | 44 | DB3+ | Digital Input Bit 3–True |
| 5 | CLK+ | Clock Input–True | 45 | DB3– | Digital Input Bit 3–Complement |
| 6 | CLK– | Clock Input–Complement | 46 | DB2+ | Digital Input Bit 2–True |
| 7 | CLKGND | Clock Supply Common | 47 | DB2– | Digital Input Bit 2–Complement |
| 8 | DGND | Digital Common | 48 | DB1+ | Digital Input Bit 1–True |
| 9 | DVDD | Digital Supply Voltage | 49 | DB1– | Digital Input Bit 1–Complement |
| 10 | DB15+ | Digital Input Bit 15–True | 50 | DB0+ | Digital Input Bit 0–True |
| 11 | DB15– | Digital Input Bit 15–Complement | 51 | DB0– | Digital Input Bit 0–Complement |
| 12 | DB14+ | Digital Input Bit 14–True | 52 | DVDD | Digital Supply Voltage |
| 13 | DB14– | Digital Input Bit 14–Complement | 53 | DGND | Digital Common |
| 14 | DB13+ | Digital Input Bit 13–True | 54 | SDO/SYNC_ALRM | SPI_DIS = 1: Data/Clock Synchronization Alarm |
| 15 | DB13– | Digital Input Bit 13–Complement | 55 | SDIO | SPI Serial Data Input/Output |
| 16 | DB12+ | Digital Input Bit 12–True | 56 | SCLK/SYNC_UPD | SPI_DIS = 1: Data/Clock Synchronization Update Required |
| 17 | DB12– | Digital Input Bit 12–Complement | 57 | CSB | SPI Chip Select (Active Low) |
| 18 | DB11+ | Digital Input Bit 11–True | 58 | RESET | Hardware Reset |
| 19 | DB11– | Digital Input Bit 11–Complement | 59 | REFIO | Reference Output, 1.2 V Nominal |
| 20 | DBVDD | Digital Data Supply Voltage | 60 | FSADJ | Full-Scale Current Adjust |

| Pin No. | Name | Description | Pin No. | Name | Description |
|---|---|---|---|---|---|
| 21 | DBGND | Digital Data Supply Common | 61 | DDR | SPI_DIS = 1: Double Data Rate Mode (Active High) |
| 22 | DB10+ | Digital Input Bit 10–True | 62 | ADVDD | Analog Supply Voltage |
| 23 | DB10– | Digital Input Bit 10–Complement | 63 | ADGND | Analog Supply Common |
| 24 | DB9+ | Digital Input Bit 9–True | 64 | ACVDD | Analog Supply Voltage |
| 25 | DB9– | Digital Input Bit 9–Complement | 65 | ACGND | Analog Supply Common |
| 26 | DB8+ | Digital Input Bit 8–True | 66 | AVDD2 | Analog Supply Voltage |
| 27 | DB8– | Digital Input Bit 8–Complement | 67 | AGND2 | Analog Supply Common |
| 28 | DATACLK_OUT+ | Data Clock Output–True | 68 | AVDD1 | Analog Supply Voltage |
| 29 | DATACLK_OUT– | Data Clock Output–Complement | 69 | AGND1 | Analog Supply Common |
| 30 | DBVDD | Digital Data Supply Voltage | 70 | IOUTB | DAC Current Output–Complement |
| 31 | DBGND | Digital Data Supply Common | 71 | IOUTA | DAC Current Output–True |
| 32 | DATACLK_IN+ | Data Clock Input–True | 72 | AGND1 | Analog Supply Common |
| 33 | DATACLK_IN– | Data Clock Input–Complement | 73 | AVDD1 | Analog Supply Voltage |
| 34 | DB7+ | Digital Input Bit 7–True | 74 | AGND2 | Analog Supply Common |
| 35 | DB7– | Digital Input Bit 7–Complement | 75 | AVDD2 | Analog Supply Voltage |
| 36 | DB6+ | Digital Input Bit 6–True | 76 | ACGND | Analog Supply Common |
| 37 | DB6– | Digital Input Bit 6–Complement | 77 | ACVDD | Analog Supply Voltage |
| 38 | DB5+ | Digital Input Bit 5–True | 78 | ADGND | Analog Supply Common |
| 39 | DB5– | Digital Input Bit 5–Complement | 79 | ADVDD | Analog Supply Voltage |
| 40 | DBVDD | Digital Data Supply Voltage | 80 | SPI_DIS | SPI Disable (Active High) |

# SERIAL PORT INTERFACE REGISTER MAPS

**Table 5. Mode Control via SPI Port**

| Address | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| COMMS | 00 | SDIODIR | DATADIR | SWRST | SLEEP | PDN | RESERVED[1] | RESERVED | EXREF |
| | 01 | | | | RESERVED | | | | |
| DATA | 02 | DATAFMT | DDR | DCLKPOLI | DCLKPOLO | DISDCLKO | SYNCMAN | SYNCUPD | SYNCALRM |
| | 03 | | | | RESERVED | | | | |
| | 04 | | | | RESERVED | | | | |
| | 05 | | | | RESERVED | | | | |
| | 06 | | | | RESERVED | | | | |
| | 07 | | | | RESERVED | | | | |
| | 08 | | | | RESERVED | | | | |
| | 09 | | | | RESERVED | | | | |
| | 0A | | | | RESERVED | | | | |
| | 0B | | | | RESERVED | | | | |
| | 0C | | | | RESERVED | | | | |
| VERSION | 0D | RESERVED | RESERVED | RESERVED | RESERVED | VERSION[3] | VERSION[2] | VERSION[1] | VERSION[0] |
| CALMEMCK | 0E | RESERVED | RESERVED | CALMEM[1] | CALMEM[0] | RESERVED | CALCKDIV[2] | CALCKDIV[1] | CALCKDIV[0] |
| MEMRDWR | 0F | CALSTAT | CALEN | XFERSTAT | XFEREN | SMEMWR | SMEMRD | FMEMRD | UNCAL |
| MEMADDR | 10 | MEMADDR[7] | MEMADDR[6] | MEMADDR[5] | MEMADDR[4] | MEMADDR[3] | MEMADDR[2] | MEMADDR[1] | MEMADDR[0] |
| MEMDATA | 11 | RESERVED | RESERVED | MEMDATA[5] | MEMDATA[4] | MEMDATA[3] | MEMDATA[2] | MEMDATA[1] | MEMDATA[0] |

[1] Reserved registers should be set to Logic 0 (low state) during a write operation, and masked (ignored) during a read operation.

**Table 6. SPI Register Definitions**

| Register | Bit | Direction | Default | Description |
|---|---|---|---|---|
| COMMCTRL(00) | | | | |
| SDIODIR | 7 | 1 | 0 | 0: SDIO pin configured for input only during data transfer |
| | | | | 1: SDIO pin configured for input or output during data transfer |
| DATADIR | 6 | 1 | 0 | 0: Serial data uses MSB first format |
| | | | | 1: Serial data uses LSB first format |
| SWRST | 5 | 1 | 0 | 1: Default all serial register bits, except address 00h |
| SLEEP | 4 | 1 | 0 | 1: DAC output current off |
| PDN | 3 | 1 | 0 | 1: All analog and digital circuitry, except serial interface, off |
| RESERVED | 2 | 0 | 0 | RESERVED |
| RESERVED | 1 | 0 | 0 | RESERVED |
| EXREF | 0 | 1 | 0 | 0: Internal bandgap reference |
| DATACTRL(02) | | | | |
| DATAFMT | 7 | 1 | 0 | 0: Twos complement input data format |
| | | | | 1: Unsigned binary input data format |
| DDR | 6 | 1 | 0 | 0: Single Data Rate mode |
| | | | | 1: Double Data Rate mode |
| DCLKPOLI | 5 | 1 | 0 | 0: Data latched on DATACLKIN rising edge |
| | | | | 1: Data latched on DATACLKIN falling edge |
| DCLKPOLO | 4 | 1 | 0 | 0: Data latched on DATACLKOUT rising edge |
| | | | | 1: Data latched on DATACLKOUT falling edge |
| DISDCLKO | 3 | 1 | 0 | 0: DATACLKOUT enabled |
| | | | | 1: DATACLKOUT disabled |
| SYNCMAN | 2 | 1 | 0 | 0: Automatic synchronization initiated following a SYNCALRM |
| | | | | 1: Manual synchronization needed following a SYNCALRM |

| | | | | |
|---|---|---|---|---|
| SYNCUPD | 1 | 1 | 0 | 0: Data synchronization complete<br>1: Initiate data synchronization |
| SYNCALRM | 0 | 0 | 0 | 0: Data synchronizer does not require updating<br>1: Data synchronizer requires updating |
| VERSION(0D) | | | | |
| VERSION[3:0] | [3:0] | 0 | – | Hardware version identifier |
| CALMEMCK(0E) | | | | |
| CALMEM | [5:4] | 0 | 00 | Calibration memory<br>00: Uncalibrated<br>01: Self calibration<br>10: Factory calibration<br>11: User input |
| CALCKDIV | [2:0] | 1 | 000 | Calibration clock divide ratio from channel data rate<br>000:/32<br>001:/64<br>110:/2048<br>111:/4096 |
| MEMRDWR(0F) | | | | |
| CALSTAT | 7 | 0 | 0 | 0: Self Calibration cycle not complete<br>1: Self Calibration cycle complete |
| CALEN | 6 | 1 | 0 | 1: Self Calibration in progress |
| XFERSTAT | 5 | 0 | 0 | 0: Factory memory transfer not complete<br>1: Factory memory transfer complete |
| XFEREN | 4 | 1 | 0 | 1: Factory memory transfer in progress |
| SMEMWR | 3 | 1 | 0 | 1: Write static memory data from external port |
| SMEMRD | 2 | 1 | 0 | 1: Read static memory to external port |
| FMEMRD | 1 | 1 | 0 | 1: Read factory memory data to external port |
| UNCAL | 0 | 1 | 0 | 1: Use uncalibrated |
| MEMADDR(10) | | | | |
| MEMADDR | [7:0] | I/O | 00000000 | Address of factory or static memory to be accessed |
| MEMDATA(11) | | | | |
| MEMDATA | [5:0] | I/O | 000000 | Data for factory or static memory access |

1: External reference

# DEFINITIONS

### Linearity Error (Also Called Integral Nonlinearity or INL)

Linearity error is defined as the maximum deviation of the actual analog output from the ideal output, determined by a straight line drawn from zero-scale to full-scale.

### Differential Nonlinearity ( DNL)

DNL is the measure of the variation in analog value, normalized to full-scale, and associated with a 1 LSB change in digital input code.

### Monotonicity

A D/A converter is monotonic if the output either increases or remains constant as the digital input increases.

### Offset Error

The deviation of the output current from the ideal of zero is called offset error. For $I_{OUTA}$, 0 mA output is expected when the inputs are all 0s. For $I_{OUTB}$, 0 mA output is expected when all inputs are set to 1s.

### Gain Error

The difference between the actual and ideal output span. The actual span is determined by the output when all inputs are set to 1s, minus the output when all inputs are set to 0s.

### Output Compliance Range

The range of allowable voltage at the output of a current-output DAC. Operation beyond the maximum compliance limits may cause either output stage saturation or breakdown, resulting in nonlinear performance.

### Temperature Drift

Temperature drift is specified as the maximum change from the ambient (25°C) value to the value at either $T_{MIN}$ or $T_{MAX}$. For offset and gain drift, the drift is reported in ppm of full-scale range (FSR) per degree celsius. For reference drift, the drift is reported in ppm per degree celsius.

### Power Supply Rejection

The maximum change in the full-scale output as the supplies are varied from minimum to maximum specified voltages.

### Settling Time

The time required for the output to reach and remain within a specified error band about its final value, measured from the start of the output transition.

### Glitch Impulse

Asymmetrical switching times in a DAC give rise to undesired output transients that are quantified by a glitch impulse. It is specified as the net area of the glitch in pV-s.

### Spurious-Free Dynamic Range

The difference, in decibels, between the rms amplitude of the output signal and the peak spurious signal over the specified bandwidth.

### Total Harmonic Distortion

THD is the ratio of the rms sum of the first six harmonic components to the rms value of the measured fundamental. It is expressed as a percentage or in decibels (dB).

### Signal-to-Noise Ratio (SNR)

S/N is the ratio of the rms value of the measured output signal to the rms sum of all other spectral components below the Nyquist frequency, excluding the first six harmonics and dc. The value for SNR is expressed in decibels.

### Adjacent Channel Power Ratio (or ACPR)

A ratio in dBc between the measured power within a channel relative to its adjacent channel.

### LVDS

Low voltage differential signaling. A differential logic specification that defines logic levels as approximately ±350 mV (differential) over a common mode range of 0.875 V to 1.575 V. LVDS is designed to achieve clock rates of up to 840 MHz.

# TYPICAL PERFORMANCE CURVES

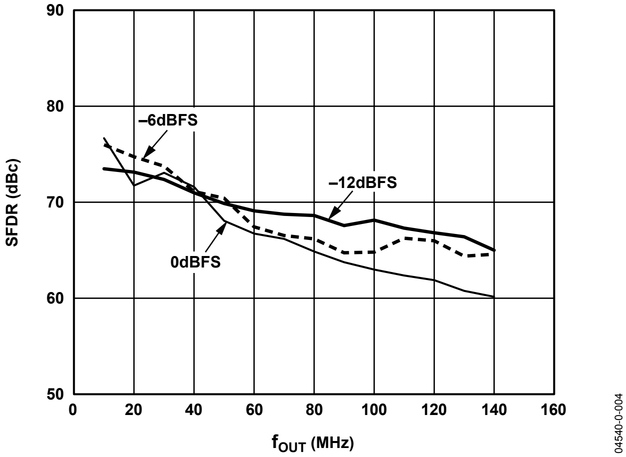


Figure 5. SFDR vs. $f_{OUT}$ at $f_{DAC}$ = 400 MSPS

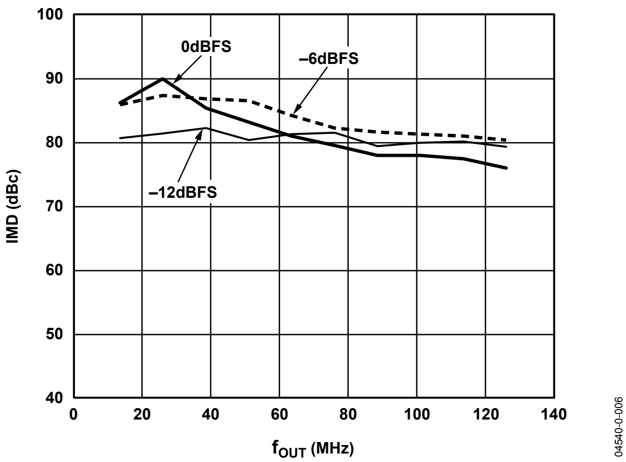


Figure 6. IMD vs. $f_{OUT}$ at $f_{DAC}$ = 500 MSPS

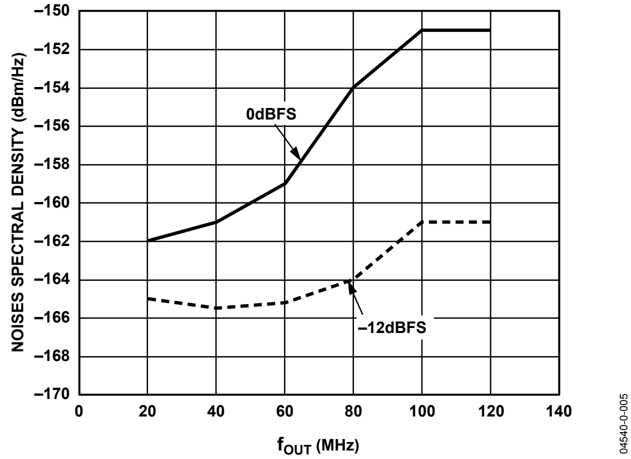


Figure 7. Noise Spectral Density vs. $f_{OUT}$ at $f_{DAC}$ = 500 MSPS

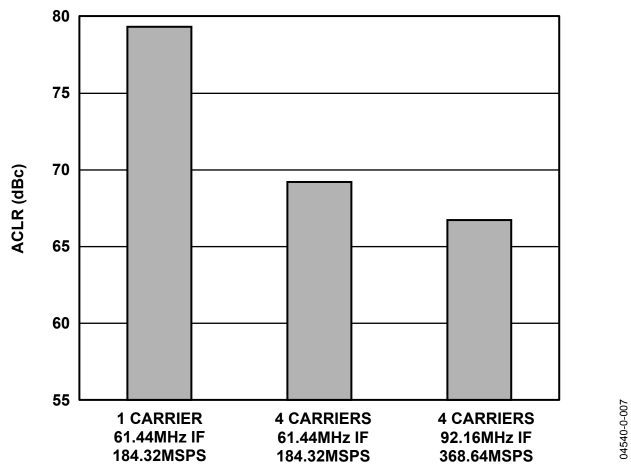


Figure 8. WCDMA ACLR at Select Intermediate Frequencies and Sample Rates

# THEORY OF OPERATION

## LVDS INPUTS

The AD9726 uses LVDS (Low Voltage Differential Signaling) digital inputs to enable high speed digital signaling. LVDS allows the use of a differential signal for optimum noise rejection, and has small signal amplitude for fast speed and lower power dissipation. Each differential digital input on the AD9726 has an internal 100 Ω resistor for proper load termination. The LVDS digital data inputs on the AD9726 meet the IEEE reduced range (RR) specs for common mode input range (875 mV to 1575 mV) with an input differential threshold of ±350 mV.

## DATA SYNCHRONIZATION CIRCUITRY

The high speeds at which the LVDS digital interface is designed to operate require maintaining synchronization of the data (DB[15:0]+, DB[15:0]−) and data clock (DATACLK_IN+, DATACLK_IN−) with the DAC clock (CLK+, CLK−). Since the DAC clock input is not LVDS, the phase relationship between that clock and the data can vary, and, unless precautions are taken, data can be corrupted.

The input data must be provided at the same frequency as the DAC clock from an LVDS source with an accompanying LVDS data clock. Since the DAC and data clocks are different types, their phase relationship is difficult to specify.

The AD9726 provides internal circuitry to keep the data from being corrupted over a wide variation in relative phase. Once the DAC and data clocks have been established and synchronization has been initiated, the phase between the two clocks can vary by at least one full clock cycle without loss of data. If the phase relationship between the clocks varies enough to cause a possible loss of data, the AD9726 can be resynchronized in several different ways.

The internal synchronization circuitry in the AD9726 eases this problem by allowing the phase to vary by at least one full clock cycle, once synchronization has been established. It does this by demultiplexing the incoming data stream into four channels, each containing every fourth data word. Each of these words is present for four DAC clock cycles. The data is then remultiplexed by sampling each channel with the appropriate DAC clock cycle.

Initial synchronization is established in one of the following ways:

1. When the RESET pin is asserted, the synchronization logic is initiated to provide optimal internal timing.
2. If SPI_DIS is not asserted, the synchronization is optimized by writing setting SYNC_UPD (02h[1]) high.
3. If SPI_DIS is asserted, the synchronization is optimized by asserting the SYNC_UPD pin.

Once synchronization is established, the AD9726 needs to be reoptimized only if operating conditions change enough to affect the relative phase of the DAC and data clocks by more than one clock cycle. The AD9726 detects when a synchronization update is necessary, and indicates this need by asserting SYNCALRM (02h[0]) or SYNC_ALRM high. If SYNCALRM (02h[0]) or SYNC_ALRM have been asserted, resynchronization can be accomplished as follows:

1. If the synchronization logic is in automatic mode (SYNCMAN (02h[2]) = 0), the synchronization logic will optimize the internal timing as necessary. Two data words will typically be lost or repeated when an optimization occurs. If that possibility could cause serious problems, manual operation may be required.
2. If the synchronization logic is in manual mode (SYNCMAN (02h[2]) = 1), the logic will indicate the need for an update by asserting SYNCALRM (02h[0]) high. In normal operation, a logic high on SYNCALRM (02h[0]) does not mean that data is being lost, but that conditions are close to the point where data may be lost. Optimization should be initiated by setting SYNCUPD (02h[1]) high at a convenient time.
3. Monitoring the synchronization logic state and initiating an update can be done via package pins by setting SPI_DIS high and using the SYNC_ALRM and SYNC_UPD pins in the same way the manual synchronization operation is described in step 2.

Note that SYNCUPD (02h[1]) or SYNC_UPD can be asserted at any time to optimize the synchronization, even if SYNCALRM (02h[0]) or SYNC_ALRM have not indicated that it is necessary.

If either the data clock or the DAC clock is interrupted for any reason, a SYNCUPD or SYNC_UPD should be executed to insure that no subsequent data is lost.

## INTERNAL REFERENCE AND FULL-SCALE OUTPUT CURRENT

The AD9726 contains an internal band gap reference of 1.2 V. The reference voltage is applied to an external resistor at FSADJ, and the resultant current is amplified by the reference buffer to provide the full-scale current for the DAC output. The gain equation from the internal reference to the DAC output (assuming the digital inputs are at full scale) is as follows:

$$I_{OUTFS} = 1.2 \times 32/FSADJ$$

Taking into account the state of the digital inputs, the output current of $I_{OUTA}$ and $I_{OUTB}$ at any instant in time is:

$$I_{OUTA} = I_{OUTFS} \times (DB15{:}DB0)/65536$$
$$I_{OUTB} = I_{OUTFS} \times (1 - DB15{:}DB0)/65536$$

## ANALOG OUTPUT

The analog output of the AD9726 is based around a high dynamic range CMOS DAC core. The output consists of a differenttial current source capable of up to 20 mA full-scale. The output devices are PMOS and are capable of sourcing current into an output termination within a compliance voltage range of ±1 V. Excellent distortion, noise, and ACLR perfor-mance is achievable to Nyquist at sample rates of 600 MSPS+.

## SPI PORT CONTROL

The AD9726 serial port is a flexible, synchronous serial communications port allowing easy interface to many industry standard microcontrollers and microprocessors. The serial I/O is compatible with most synchronous transfer formats, including both the Motorola SPI and Intel SSR protocols. The interface allows read/write access to all registers that configure the AD9726. Single or multiple byte transfers are supported as well as MSB first or LSB first transfer formats. The AD9726 serial interface port can be configured as a single pin I/O (SDIO) or two unidirectional pins for in/out (SDIO/SDO).

## GENERAL OPERATION OF THE SERIAL PORT INTERFACE

There are two phases to a communication cycle with the AD9726. Phase 1 is the instruction cycle, which is the writing of an instruction byte into the AD9726, and coincident with the first eight SCLK rising edges. The instruction byte provides the AD9726 serial port controller with information regarding the data transfer cycle, which is Phase 2 of the communication cycle. The Phase 1 instruction byte defines the number of bytes in the data transfer, the starting register address for the first byte of the data transfer, and whether the upcoming data transfer is read or write. The first eight SCLK rising edges of each communication cycle are used to write the instruction byte into the AD9726.

A Logic 1 on the CS pin followed by a Logic 0 will reset the SPI port timing to the initial state of the instruction cycle. This is true regardless of the present state of the internal registers or the other signal levels present at the inputs to the SPI port. If the SPI port is in the midst of an instruction cycle or a data transfer cycle, none of the present data will be written.

The remaining SCLK edges are for Phase 2 of the communication cycle. Phase 2 is the actual data transfer between the AD9777 and the system controller. Phase 2 of the communication cycle is a transfer of 1, 2, 3, or 4 data bytes as determined by the instruction byte. Normally, using one multibyte transfer is the preferred method. However, single byte data transfers are useful to reduce CPU overhead when register access requires 1 byte only. Registers change immediately upon writing to the last bit of each transfer byte.

## INSTRUCTION BYTE

The instruction byte contains the information shown in Table 7

**Table 7**

| N1 | N0 | Description |
|---|---|---|
| 0 | 0 | Transfer 1 byte |
| 0 | 1 | Transfer 2 byte |
| 1 | 0 | Transfer 3 byte |
| 1 | 1 | Transfer 4 byte |

### *R/W*

Bit 7 of the instruction byte determines whether a read or a write data transfer will occur after the instruction byte write. Logic high indicates a read operation. Logic 0 indicates a write operation. N1, N0 -Bits 6 and 5 of the instruction byte determine the number of bytes to be transferred during the data transfer cycle. The bit decodes are shown in the following table:

**Table 8**

| MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| I7<br>R/W | I6<br>N1 | I5<br>N0 | I4<br>A4 | I3<br>A3 | I2<br>A2 | I1<br>A1 | I0<br>A0 |

### *A4, A3, A2, A1, A0*

Bits 4, 3, 2, 1, 0 of the instruction byte determine which register is accessed during the data transfer portion of the communications cycle. For multibyte transfers, this address is the starting byte address. The remaining register addresses are generated by the AD9726.

## SERIAL PORT INTERFACE PIN DESCRIPTION

### *SCLK (Serial Clock)*

The serial clock pin is used to synchronize data to and from the AD9726, and to run the internal state machines. The SCLK maximum frequency is 15 MHz. All data input to the AD9726 is registered on the rising edge of SCLK. All data is driven out of the AD9726 on the falling edge of SCLK.

### *CSB (Chip Select)*

Active low input starts and gates a communication cycle. It allows more than one device to be used on the same serial communications line. The SDO and SDIO pins will go to a high impedance state when this input is high. Chip select should stay low during the entire communication cycle.

### *SDIO*

Serial data I/O. Data is always written into the AD9726 on this pin. This pin, however, can be used as a bidirectional data line. The configuration of this pin is controlled by Bit 7 of register address 00h. The default is Logic 0, which configures the SDIO pin as unidirectional.

### SDO

Serial data out. Data is read from this pin for protocols that use separate lines for transmitting and receiving data. In the case where the AD9726 operates in a single bidirectional I/O mode, this pin does not output data and is set to a high impedance state.

### MSB/LSB Transfers

The AD9726 serial port can support both MSB first and LSB first data formats. This functionality is controlled by register address 00h Bit 6. The default is MSB first. When this bit is set to active high, the AD9726 serial port is in LSB first format. That is, if the AD9726 is in LSB first mode, the instruction byte must be written from least significant bit to most significant bit. Multibyte data transfers in MSB format can be completed by writing an instruction byte that includes the register address of the most significant byte. In MSB first mode, the serial port internal byte address generator decrements for each byte required of the multibyte communication cycle. Multibyte data transfers in LSB first format can be completed by writing an instruction byte that includes the register address of the least significant byte. In LSB first mode, the serial port internal byte address generator increments for each byte required of the multibyte communication cycle.

The AD9726 serial port controller address will increment from 1Fh to 00h for multibyte I/O operations if the MSB first mode is active. The serial port controller address will decrement from 00h to 1Fh for multibyte I/O operations if the LSB first mode is active.

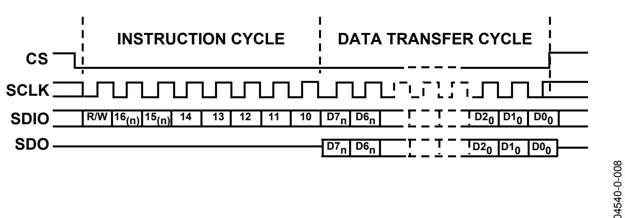


Figure 9. Serial Register Interface Timing MSB First

## NOTES ON SERIAL PORT OPERATION

The AD9726 serial port configuration bits reside in Bit 6 and Bit 7 of register address 00h. It is important to note that the configuration changes immediately upon writing to the last bit of the register. For multibyte transfers, writing to this register may occur during the middle of communication cycle. Care must be taken to compensate for this new configuration for the remaining bytes of the current communication cycle.

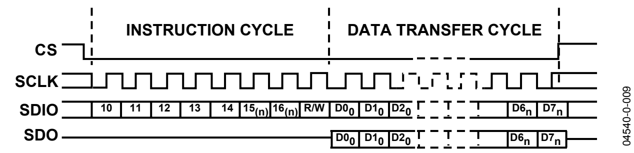


Figure 10. Serial Register Interface Timing LSB First

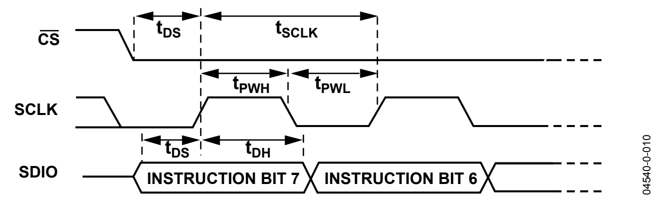


Figure 11. Timing Diagram for Register Write to AD9726

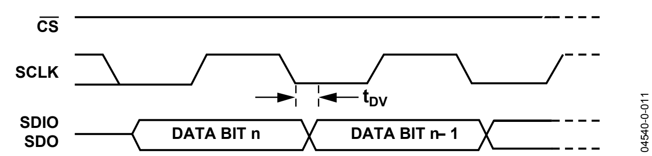


Figure 12. Timing Diagram for Register READ to AD9726

The same considerations apply to setting the reset bit in register address 00h. All other registers are set to their default values, but the software reset doesn't affect the bits in register address 00h.

It is recommended to use only single byte transfers when changing serial port configurations or initiating a software reset.

# OUTLINE DIMENSION

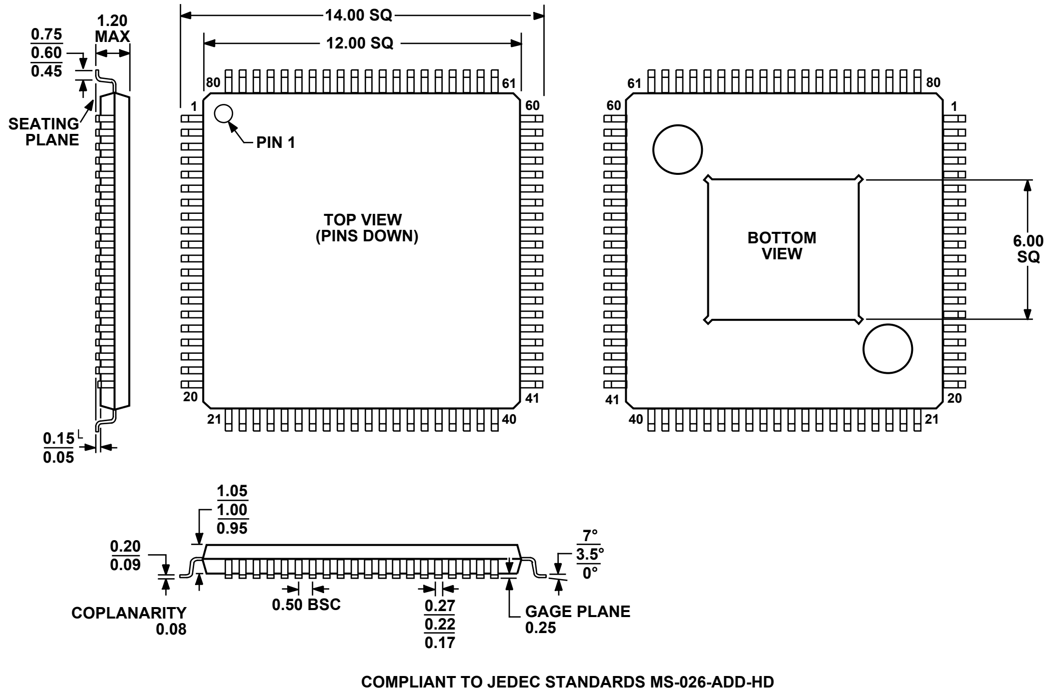


*Figure 13. 80-Lead Thin Plastic Quad Flat Package, Exposed Pad [TQFP/ED]*
*(SV-80)*
*Dimensions shown in millimeters*

## ORDERING GUIDE

| Model | Temperature Range | Package Description | Package Option |
|---|---|---|---|
| AD9726BSV | -40°C to +85°C | 80 Lead TQFP | SV-80 |

### THERMAL CHARACTERISTICS

Thermal Resistance
80-Lead Thermally Enhanced
TQFP Package $\theta_{JA}$ = 23.5°C/W*

*With thermal pad soldered to PCB.


PR04540-0-1/04(PrD)